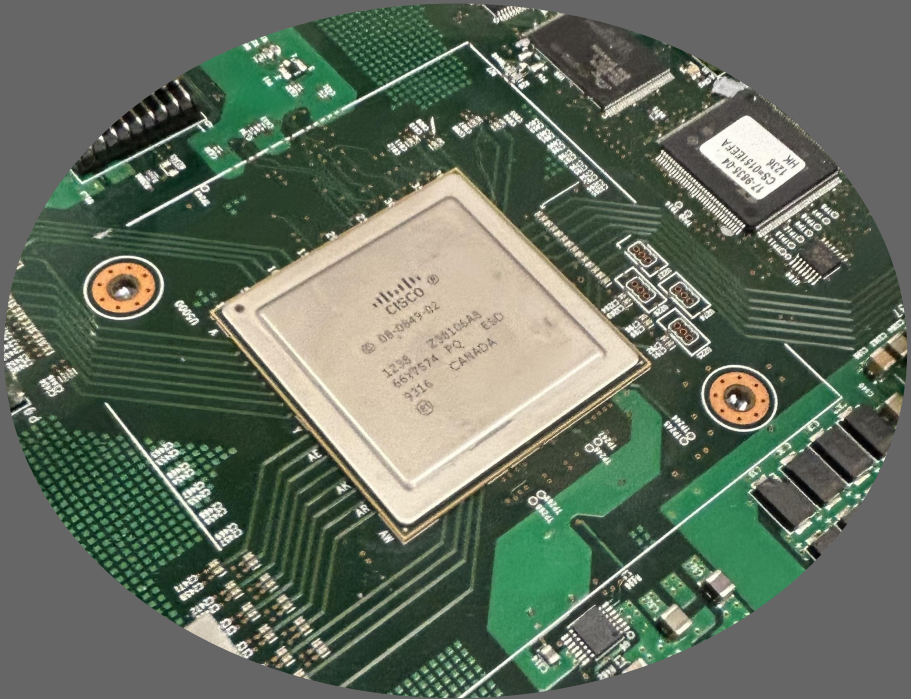


CPE 470 - Open Source ASIC Design

Taught by Francisco Wilken



What is the Goal?

- Design an **ASIC**!
 - Basically a chip that solves a specific problem really well
- **RTL** Design of System
 - Describe system using **HDL**
 - HDL is the specific language used
 - In our case **System Verilog**
- Simulate and Validate Design
- Use **EDA** tools to turn RTL into manufacturable product

Glossary

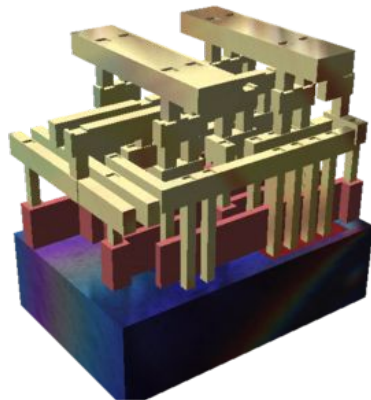
ASIC: Application Specific Integrated Circuit

RTL: Register Transfer Layer

HDL: Hardware Description Language

EDA: Electronics Design Automation

3D Visualization of
Manufacturable File

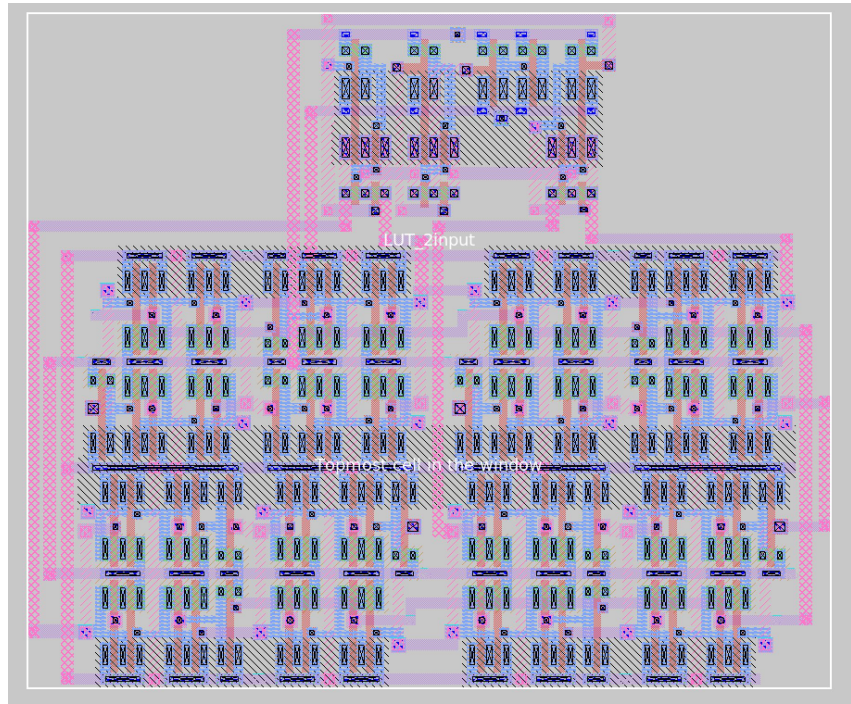


Why Not FPGAs?

- FPGAs are great prototyping tools!
 - Also used extensively in products

However...

- Re-Configurable **LookUp Table (LUT)** takes ~**200** transistors
- Static Logic Gates generally take **2-12 transistors**
- Static Gates are ~**20 times smaller**



FPGA vs ASIC Tradeoffs

	FPGA	ASIC
Development Cost	Low	High
Unit Price	High	Low
Speed	Medium	High
Logic Density	Low	High

Fabs and Foundries

Glossary

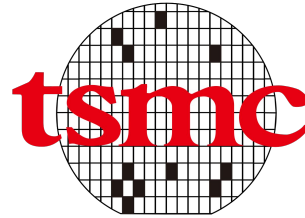
Fab: Factory or plant that makes chips

Foundry: Company that makes chips for others

Tape Out: Send final design to get fabricated

- Chips have to be specifically designed for a certain manufacturer
- Once designed, send to **foundry**
 - Sending off your design is called a **Tape-Out**
 - Named after sending physical tapes of design files

Industry Foundries



Open Source Foundries



Process Nodes and PDKs

Glossary

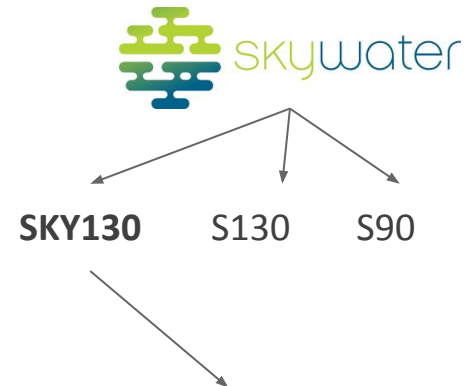
PDK: Process Design Kit

Process Node: a specific semiconductor manufacturing process

- Characterized by gate length, I.E. 130 nm
- Each Foundry has multiple process nodes at varying sizes and prices

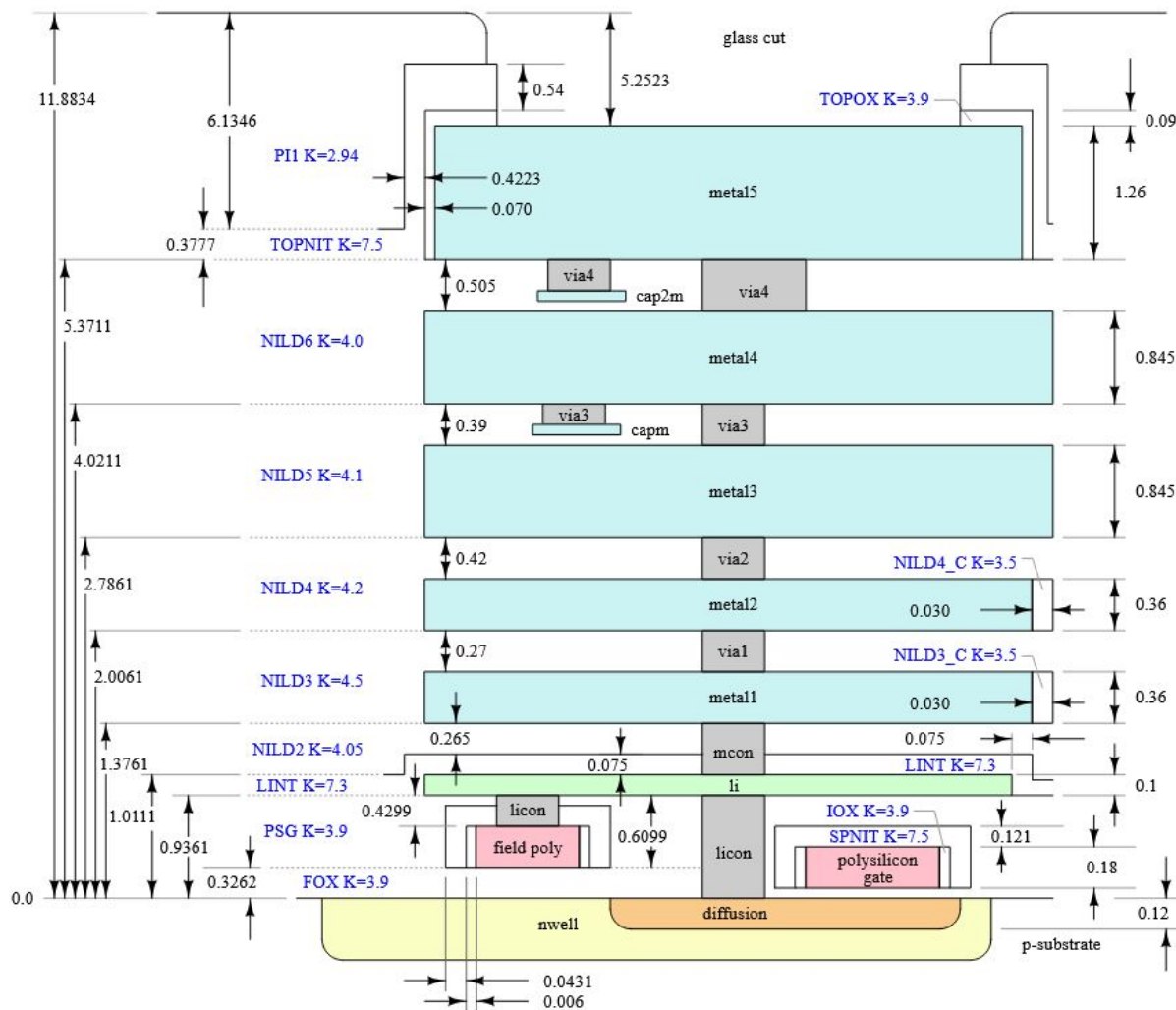
Foundry provides a **PDK** for each of their Process Nodes:

- Technology Information:
 - Available Layers
 - Electrical Rules
 - Design Constraints
- Device Primitives
 - Base-level Transistors
 - Models of
- Standard Cells
 - Standardized Logic Gates



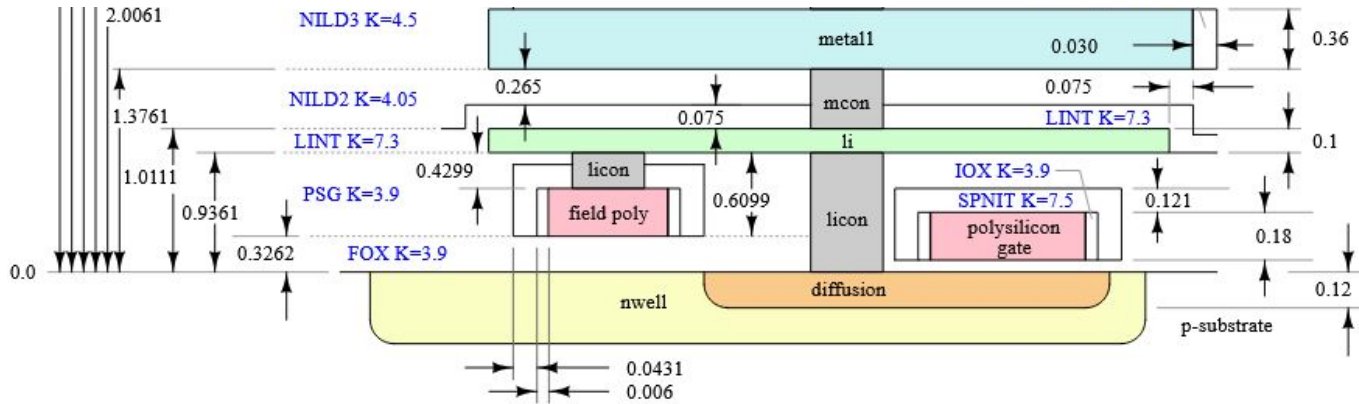
Tech Info, Standard Cells, Devices

Skywater 130nm Stackup



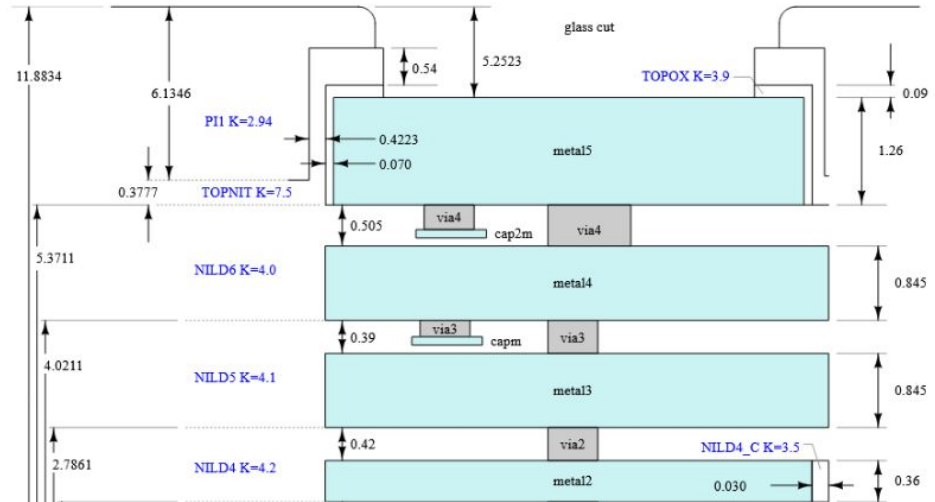
Bottom Layers: Gates

- Bottom layers are used to create logic gates
 - Substrate, Well, Diffusion, and Polysilicon Gate used to create transistors
 - Local Interconnect (LI) used to connect transistors into logic gates
- Low-numbered Metal used to create:
 - power and ground rails
 - contacts for inputs and outputs of logic gates



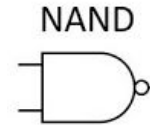
Top Metal Layers: Power and Routing

- Thicker Top Layers
 - Better current conduction
 - Power and Ground Distribution
- Middle Layers used to route:
 - Clocks
 - Global signals
 - Connect Distant Gates
- **Vias** used to move between metal layers

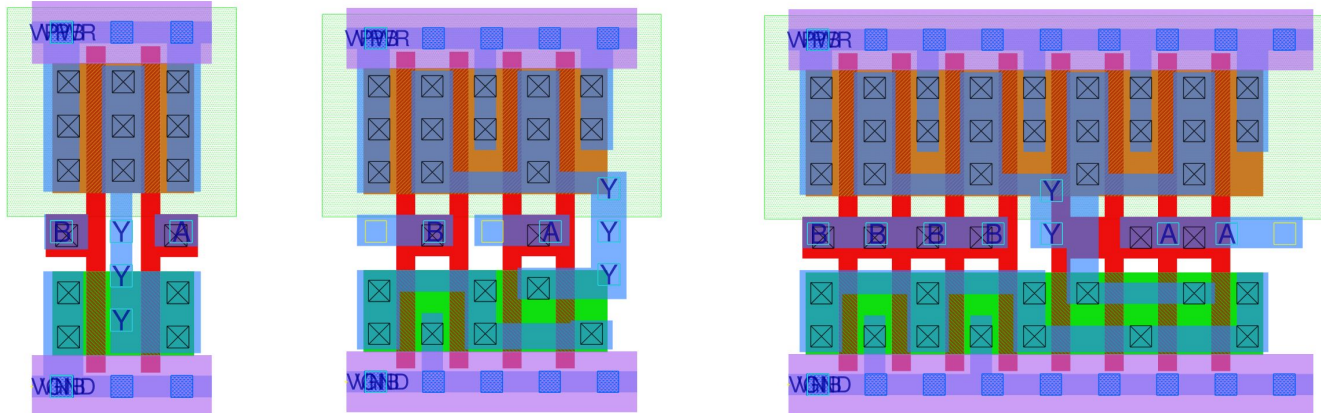


Standard Cells

- Is an implementation of a standard logic function
 - For example: NAND (Not And)
 - Designed and tested by the Foundry
- Come in multiple sizes depending on drive strength
 - Drives Many Other Gates -> Larger
 - Drives Few Gates -> Smaller

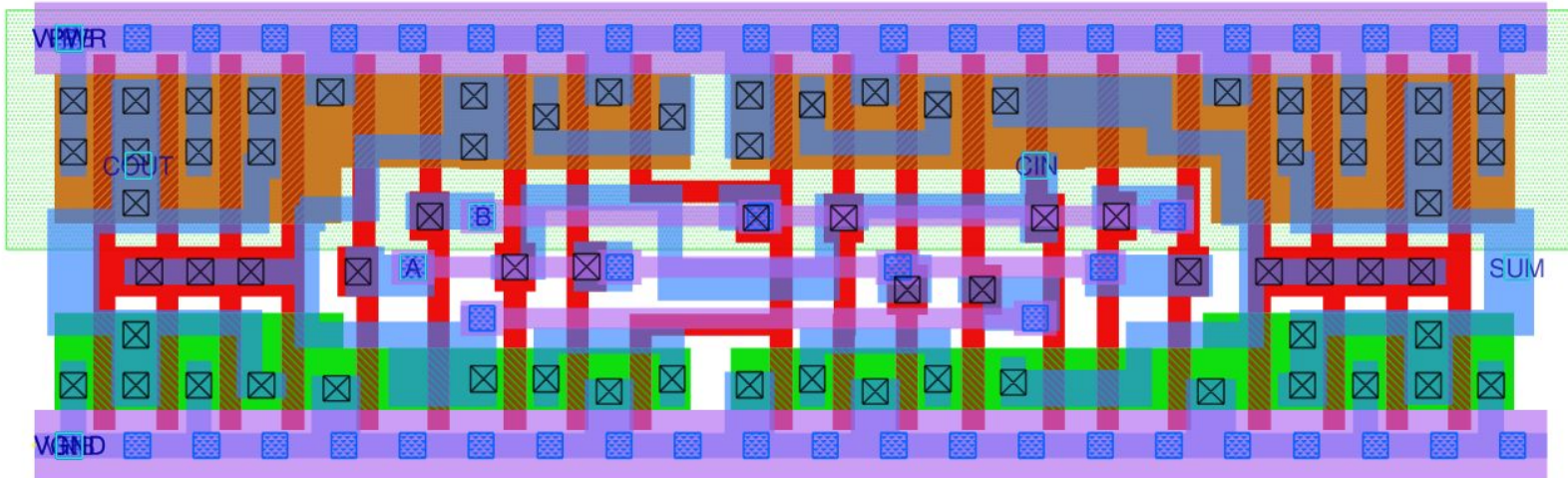
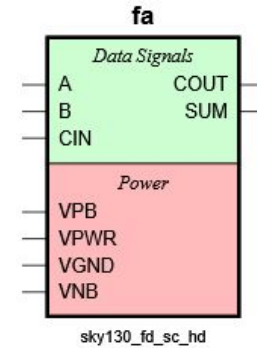


A	B	Output
0	0	1
1	0	1
0	1	1
1	1	0



Larger Standard Cells

- Vary in complexity:
 - **Inverter** -> Simplest Standard Cell
 - **Full Adder** -> More Complex Standard Cell
- Not all just simple boolean functions



Standard Cell Nomenclature

sky130_fd_sc_hd_nand2

Process: Skywater 130nm

Source: Foundry (Skywater)

Type: Standard Cell

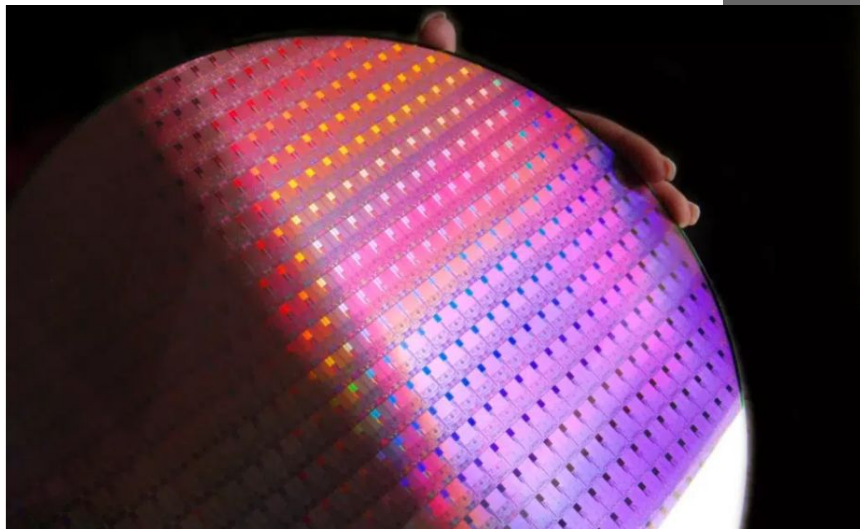
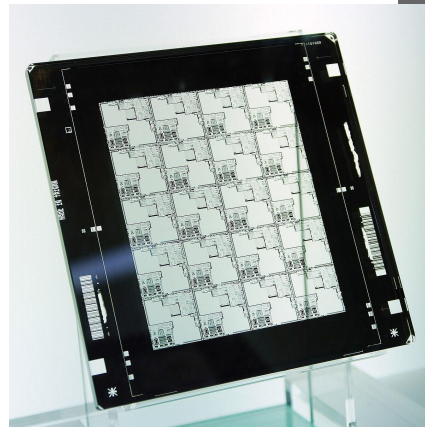
Library: High Density

Cell: 2-Input NAND

<Process name> _ <Library Source Abbreviation> _ <Library Type Abbreviation> [_ <Library Name>]

Fabrication Time

- Chips are mass produced on silicon wafers
 - Standard 12-inch wafer can fit ~300 chips
- Manufactured using masks for each layer of chip
 - Masks are expensive to produce but highly reusable
 - High Up-Front Cost, Low Unit Cost
- High Volume, Long Turnaround Time
 - Tape Outs can take 6+ months

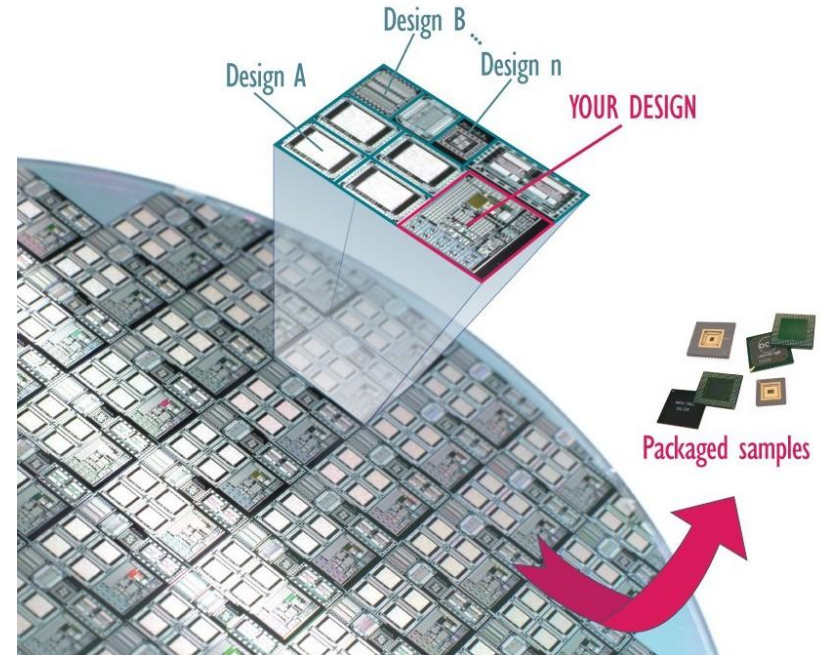


Multi Project Wafers

Glossary

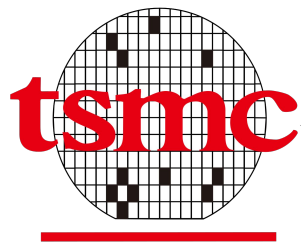
MPW: Multi Project Wafer

- Buying an entire wafer of chips is ridiculously expensive
 - What if multiple people's designs could fit on one wafer?
- Enter **MPW** companies
 - Aggregate the designs of many parties
 - Combine into large mask
 - Work closely with foundry
 - Profit?
- MPW programs also handle some difficulties:
 - Packaging Chips:
 - Raw Silicon -> Package with Pins
 - Analog Circuitry:
 - Driving IO Pins
 - Managing Power

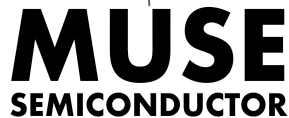


MPW Landscape

Foundry



MPW
Middleman



End Users



MPW Issues

- Most MPW services are still too expensive for educational use
- E-Fabless going out of business took away the cheapest option



• The MOSIS Service invoices the Registration Fee

There is a \$10,000 Registration fee

Please note the minimum fabrication order is \$25,000

MUSE SEMICONDUCTOR

It's not just an MPW.

Min. Area (mm²) 25

Frequency Monthly

Cycle Time (days) 42

Sample Qty. 40

Price (\$/mm²) 1,000



Now What?

Come back next time for future plans in education level tape outs.



References

- <https://skywater-pdk.readthedocs.io/en/main/>
- <https://themosisservice.com/>
- https://en.wikichip.org/wiki/technology_node
-

The major ASIC-related factors that affect system partitioning with ASICs are:

- maximum die size
- type of ASIC design
- speed requirements
- type of logic
- power dissipation
- I/O per chip available